REMARKS

Claims 10-15 and 17-34 are pending in this application. By the Office Action, claims 10-34 are rejected under 35 U.S.C. §103. By this Amendment, claims 10 and 24 are amended. Claim 10 is amended in part by incorporating the subject matter of claim 16, which is canceled without prejudice to or disclaimer of the subject matter recited in that claim. No new matter is introduced through these amendments.

Support for the amendments can be found in the specification as filed. See pages 14 and 16-18. Reconsideration of the application in view of the above amendments and the following remarks is respectfully requested.

I. Rejections Under 35 U.S.C. §103

a. Claims 10, 11, 14 and 20

The Office Action rejects claims 10, 11, 14 and 20 under 35 U.S.C. §103(a) as being unpatentable over Wise (JP 09-120947) (hereinafter "Wise") in view of Satoshi (JP 10-106955) (hereinafter "Satoshi"). Applicants respectfully traverse the rejection.

By this Amendment, independent claim 10 is amended, in part by incorporating the subject matter of claim 16, which is canceled without prejudice to or disclaimer of the subject matter recited in that claim. Independent claim 10 specifies, *inter alia,* a method for producing a silicon epitaxial wafer comprising a sub-epitaxial layer forming step, the sub-epitaxial layer not including the dopant, and a time within 60 minutes of exposing the silicon single crystal substrate to air between the hydrofluoric acid treating step and the baking step.

In the instant application, the sub-epitaxial layer or cap-layer growth is formed on the main surface of the substrate at a low temperature to prevent dopant that was added to the substrate from being discharged into the chamber. (See p. 17). After formation of the sub-epitaxial layer, the main epitaxial layer is formed. Because the dopants are scarcely discharged into vapor phase during heat treatment in the baking step, the vapor phase growth

of the main epitaxial layer is formed with a more precipitous impurity profile and as a result the transition width of the epitaxial layer is considerably narrowed. (See p. 19). The cited references, alone or in combination, fail to teach or suggest a method for producing a silicon epitaxial wafer as claimed above and thus as a result, the references thus would not have rendered obvious the claimed invention.

Wise teaches a method for forming an epitaxial layer wherein the substrate is heated to a high temperature so that the natural oxide film is removed, and then subsequently the growth of the epitaxial layer is completed at that temperature. (Wise translation, p. 3; "temperature of an epitaxial [deposition] room is made high to the temperature...for carrying out the deposit of the remainder of an epitaxial layer.") As a result of this, the transition width of the epitaxial layer is comparatively wider or less narrow as a result of an auto-doping phenomenon. However, nowhere does Wise teach or suggest a cap layer growing performed on the main surface of the substrate at a low temperature so as to prevent the dopant added to the substrate from being discharged into the chamber, as claimed.

In addition, Wise further fails to teach or suggest a time of within 60 minutes of exposing the silicon single crystal substrate to air between the acid treating step and the baking step, as recited in independent claim 10.

Satoshi does not overcome the deficiencies of Wise. Satoshi teaches a method of manufacturing a semiconductor substrate wherein a blocking film is formed on the substrate. (Satoshi translation; abstract). However, nowhere does Satoshi teach or suggest a method for producing a silicon epitaxial wafer wherein the sub-epitaxial layer or cap-layer growth is formed on the main surface of the substrate at a low temperature to prevent dopant that was added to the substrate from being discharged into the chamber, nor teach or suggest a time of within 60 minutes of exposing the silicon single crystal substrate to air between the acid treating step and the baking step, as claimed.

In view of the foregoing, neither Wise nor Satoshi, alone or in combination, can reasonably be considered to teach or suggest the method for producing a silicon epitaxial wafer, as claimed. Neither Wise nor Satoshi teaches or suggests cap layer growing at a low temperature resulting in a considerably narrow epitaxial layer transition width, or a time within 60 minutes of expositing the substrate to air between the acid treating step and baking step. The references thus would not have rendered obvious the claimed invention.

Claims 11, 14 and 20 variously depend from independent claim 10. Because Wise and Satoshi fail to teach or suggest, alone or in combination, the features recited in independent claim 10, dependent claims 11, 14 and 20 are patentable for at least the reasons that claim 10 is patentable, as well as for the additional features they recite.

Accordingly, reconsideration and withdrawal of the rejection are respectfully requested.

b. Claims 12, 13, 15-19 and 21-34

The Office Action rejects claims 12, 13, 15-19 and 21-34 under 35 U.S.C. §103(a) as being unpatentable over Wise in view of Satoshi. Applicants respectfully traverse the rejection.

The above discussion with respect to claims 10, 11, 14 and 20 is incorporated herein by reference. Claims 12, 13, 15-19 and 21-33 variously depend from independent claim 10. Because Wise and Satoshi, alone or in combination, fail to teach or suggest the features recited in independent claim 10, dependent claims 12, 13, 15-19 and 21-22 are patentable for at least the reasons that claim 10 is patentable, as well as for the additional features they recite.

The Office Action asserts that the combined references of Wise and Satoshi disclose all features of independent claim 34 with the exception of thicknesses of the layers, time between steps, and dopant amounts. The Office Action alleges that it would have been

obvious to determine through routine experimentation the optimum values of the above variables in order to create desired properties. The analysis of the Office Action fails for at least the following reasons.

In order to assert that such purported optimization would have been obvious, the Office Action is required to first establish by specific objective evidence in the prior art that the claimed feature(s) are a result-effective variable. MPEP §2144.05. Put another way, the Office Action must provide support or evidence for why one of ordinary skill in the art would have been motivated to optimize the variable in question through added experimentation. Applicants respectfully submit that no such objective evidence of record has been demonstrated that can reasonably be considered to have suggested that thicknesses of the layers, time between steps, and dopant amounts are recognized result-effective variables with regard to the applied references.

In addition, Applicants submit evidence of unexpected results related to the features described in claim 34. Claim 34 describes, *inter alia*, a baking step comprising performing a dry etching of the silicon single crystal substrate while the substrate is heated to a temperature of 950°C or less and a time of exposing the silicon crystal substrate to air as set to within 60 minutes. Both of these features produced unexpected results as claimed.

Through maintaining the temperature during this stage of the process at 950°C or less, unexpected results were reached by decreasing the severity of the auto-doping phenomenon. From these results, it was found that by employing the method as claimed in claim 34, it is possible to perform a vapor phase growth of a silicon epitaxial later while obtaining a more precipitous dopant profile on a main surface of a silicon single crystal substrate. (See Fig. 2).

In addition, any increase to the total time of exposure of the silicon single crystal substrate to air that exceeds 60 minutes results in a non-negligible increase in an auto-doping phenomenon. (See p. 7-8).

For at least the above reasons, any combination of the cited references fails to teach or suggest, alone or in combination, all of the positively recited features in independent claim 34. The references thus would not have rendered obvious the claimed invention.

Accordingly, reconsideration and withdrawal of the rejection are respectfully requested.

II. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of the application are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

William P. Berridge
Registration No. 30,024

Joel S. Armstrong
Registration No. 36,430

WPB:SQL/mef

Attachment:
Petition for Extension of Time

Date: July 22, 2008

OLIFF & BERRIDGE, PLC
P.O. Box 320850
Alexandria, Virginia 22320-4850
Telephone: (703) 836-6400

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